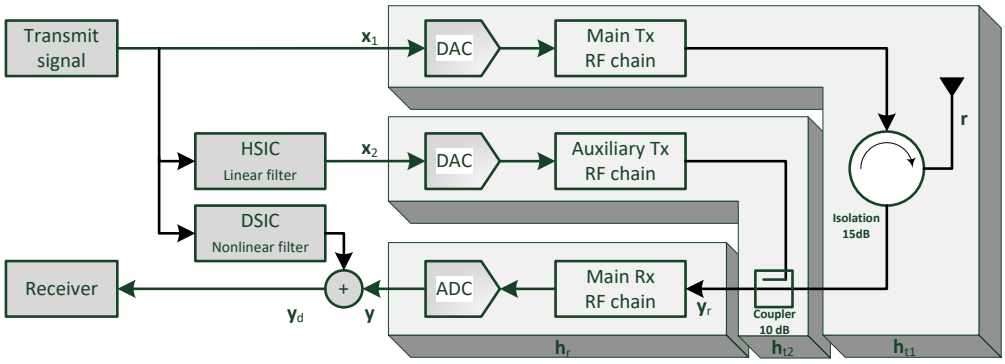
Flex5Gware year 1 golden nugget

One of the main objectives of Flex5Gware is to pin point specific implementation challenges for 5G hardware (HW) and software (SW) platforms targeting both network elements and devices. This implementation complexity analysis is used, for example, to indicate the viability of anticipated solutions for 5G. In particular, Flex5Gware is focusing on providing a proof-of-concept (PoC) of the key building blocks that 5G HW/SW platforms will be composed of. With its 11 PoCs, Flex5Gware covers the whole value chain of 5G platforms: starting from the antenna, RF modules and mixed signal stages and going up to digital HW and SW aspects.

At the end of this first year, besides producing the deliverable that contains the complete description of all Flex5Gware PoCs in terms of technology to be used, test object lists, and mapping to 5G use cases, Flex5Gware had outstanding achievements in its PoCs. Particularly, already 5 PoCs were showcased at EuCNC in Athens showing HW/SW enablers for 5G. Improvements in terms of reduced cost and footprint for the analogue hardware and increased flexibility and reduced energy techniques based on context awareness were shown at the Flex5Gware booth. Among these 5 PoCs, the Flex5Gware consortium would like to highlight as its year 1 golden nugget the “Full duplex transceiver”. The full duplex transceiver is the result of the collaboration between Intel and CEA and this technology provides gains in the user data rate of up to 50 % and in aggregated data rates (in a multiuser setting) of up to 21 % compared to settings in which full duplex is not available. Moreover, the main advantage of the work carried out in Flex5Gware with respect to prior art is that the proposed full duplex architecture is based on a conventional multiple-input multiple-output (MIMO) hardware architecture, which implies that no significant changes in the hardware will be required to endow MIMO transceivers with full duplex capabilities. A block diagram of the full duplex transceiver architecture is depicted in the figure below.



Block diagram of the self-interference cancellation architecture of the Flex5Gware full duplex transceiver